

Attorney Docket No. 103-1
Client Reference No. 0099.00US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: YING-WAI, Ho et al. Serial No.: 09/577,238 Filed: May 23, 2000 For: FLOATING-POINT PROCESSOR WITH OPERATING MODE HAVING IMPROVED ACCURACY AND HIGH PERFORMANCE	Examiner: DO, Chat C. Art Unit: 2124 INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98
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Assistant Commissioner for Patents
Washington, D.C. 20231


Sir:

The references cited on attached form PTO-1449 are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited information be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue there from.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 50-1229. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,


Truong T. Dinh
Reg. No. 40,993

DINH & ASSOCIATES 2506 Ash Street Palo Alto, California 94306 Tel: (650) 289-0600 Fax: (650) 289-0700	I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 By: <u>Truong T. Dinh</u> On: <u>February 18, 2005</u>
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FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)			Attorney Docket No.: 103-1		Application No.: 09/577,238	
			Applicant: YING-WAI, Ho et al.			
			Filing Date: May 23, 2000		Group:	
Reference Designation			U.S. PATENT DOCUMENTS			Page 1
Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
AA	5,862,066	1/19/99	Rossin et al	364	736	
AB	6,298,365	10/2/01	Dubey et al	708	495	
AC	6,401,108	6/4/02	Van Nguyen	708	671	
AD	6,581,087	6/17/03	Inoue et al	708	671	
AE	5,619,198	4/8/97	Blackham et al	341	150	
AF	6,175,907	1/16/01	Elliott et al	712	1	
AG	5,977,987	11/2/99	Duluk, Jr.	345	441	
AH	5,982,380	11/9/99	Inoue et al	345	434	
AI	6,631,392	10/7/03	Jiang et a	708	498	
AJ	6,697,832	2/24/04	Kelley et al	708	501	
AK	6,714,197	3/30/04	Thekkath et al	345	427	
AL	6,732,259	5/4/04	Thekkath et al	712	233	
FOREIGN PATENT DOCUMENTS						
	Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
AM	"MIPS Extension for Digital Media with 3D," MIPS Technologies, Inc., pp. 1-26, Dec 27, 1996.					
AN	Thekkath et al, "An Architecture Extension for Efficient Geometry Processing," pp. 1-23, Presented at Hot Chips 11, A Symposium of High-Performance Chips, Stanford Univ. (August 1999) (submitted for conference review July 14, 1999)					
AO	Uhler, M., "Optimizing Game Applications for the MIPS RISC Architecture," 1999 Computer Game Developer's Conference, San Jose, CA, 14 pages (March 1999) (submitted for conference review on 2/12/99)					
AP	Uhler, M., "Optimizing Game Applications for the MIPS RISC Architecture," 1999 Computer Game Developer's Conference, San Jose, CA, slides 1-22 (March 1999)					
AQ	Kubosawa, H. et al., "A 2.5-GFLOPS, 6.5 Million Polygons per Second, Four-Way VLIW Geometry Processor with SIMD Instructions and a Software Bypass Mechanism," IEEE Journal of Solid-State Circuits, IEEE, Vol. 34, No. 11, pp. 1619-1626, (November 1999) (appears to correspond to document AR1, Higaki, N. et al.).)					
AR	Rice et al, "Multiprecision Division on an 8-Bit Processor," Computer Arithmetic, 1997 (Proceedings, 13th IEEE Symposium on July 6-9, 1997, pp. 74-81)					
AS	Oberman et al., "AMD 3DNow! Technology and the K6-2 Microprocessor" (presentation), Proceeding Notebook for Hot Chips 10, August 16-18, 1998 (pp. 245-254).					
AT	U.S. Patent Application Serial No. 09/364,512, "Processor with Improved Accuracy for Multiply-Add Operations," Ying-wai Ho et al, filed on July 30, 1999					
AU	U.S. Patent Application Serial No. 09/363,637, "System and Method for Improving the Accuracy of Reciprocal and Reciprocal Square Root Operations Performed by a Floating-Point Unit," by Ying-wai Ho et al, filed on July 30, 1999					
AV	U.S. Patent Application Serial No. 09/364,786, entitled "Processor Having a Compare Extension of an Instruction Set Architecture," by Radhika Thekkath et al, filed on July 30, 1999					
EXAMINER			DATE CONSIDERED			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.